A New Voltage Regulator Design

Linear voltage regulators have been commodity parts for many years and are often taken for granted as a DC power source. However, like any real device they have limitations. Using a better regulator can simplify circuit design, reduce component count and enhance performance. This article discusses the patented (U.S. Patent 8,294,440). design of a new high performance regulator and its benefits.

A Basic Feedback Voltage Regulator

The basic voltage regulator shown in figure 1 has a fixed reference voltage VREF, an error amplifier A1 and an output transistor Q1. The error amplifier compares the output voltage to the reference voltage and makes them equal relative to the ratio of feedback resistors R1 and R2. VREF current is set by current source Q3. In this particular variation, Q2 is also a current source and A1 controls the load current from Q1 by sinking any base current not needed to stimulate load current from the emitter.

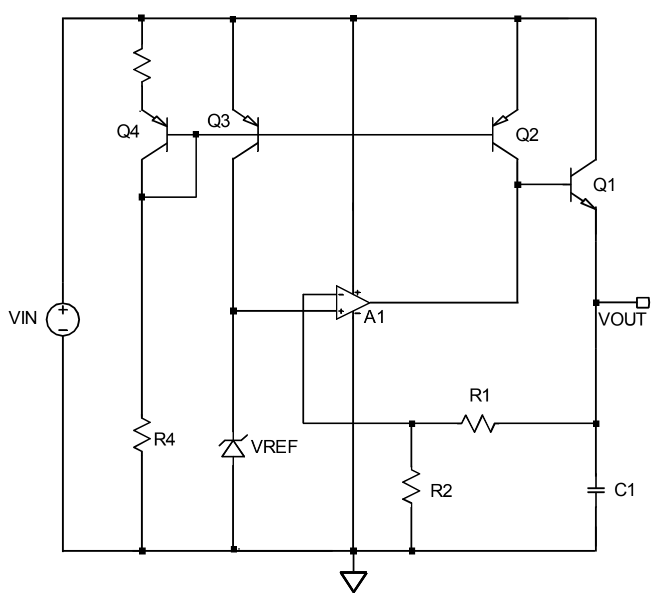

Figure 1: A basic voltage regulator topology

While this regulator is decent, it has multiple sources of error and some other limitations.

Error Sources

Power Supply Ripple Rejection of A1

First consider VIN, which has noise that the regulator attempts to remove. Noise is defined here as any deviation from perfect DC: high frequency noise coupled from a power (mains) line; ripple from a filtered rectifier; digitally induced noise from nearby circuitry; traditional Johnson noise, etc.

A1 has its power source connected directly to the noisy input voltage and any non–DC signal on VIN that eludes the supply rejection ability of A1 goes directly to VOUT via the emitter follower Q1.

The simplest form of A1 is a resistively loaded common emitter inverter. This provides decent load regulation but poor supply rejection. A differential pair provides better rejection but still suffers from finite collector impedance and Early effect degradation. These regulators typically offer 40 to 80 dB of input AC rejection at low frequencies, which decreases as frequency goes up due to junction capacitance of Q1, Q2 and Q3 and coupling from the base of Q4.

Using an op amp for A1 gives much better supply rejection at low frequency, but the PSRR of most op amps is high (110dB) at DC and rolls off rapidly as frequency increases. Interestingly, our measurements show monolithic regulators' low frequency PSRR is generally not as good as that of a typical op amp, so either their internal amplifiers are not as good or other error sources dominate.

The Early effect of Q2 and Q3 collectors causes some modulation of their currents with VIN changes. This appears at VOUT as ripple that is not rejected.

Other Error Sources

When a changing load demands more or less current, VOUT will change due to the low but finite impedance of Q1 emitter. A1 detects this difference and responds by changing Q1's base current to bring VOUT back to its expected value. The bandwidth, loop stability and possibly the slew rate of A1 determine how fast the loop responds and VOUT settles.

If VOUT = VREF, the loop gain of A1 is unity (R2 is infinite) and A1's bandwidth is maximized, assuming A1 is a transconductance amp. If VOUT > VREF, the bandwidth of A1 decreases proportionally and the settling time of VOUT increases.

Practical Drawbacks

Notice the basic regulator has the full VIN across A1. This limits VIN to the amplifier's maximum voltage range, often preventing the use of newer low voltage high performance op amps.

For full closed loop regulation, the basic regulator requires Q1 and Q2 to operate in their linear (non-saturated) region. Thus the minimum operating voltage between VIN and Q1's emitter sets the minimum VIN for regulation. This is the "drop out voltage" and for the basic regulator in figure 1 consists of VBE of Q1 and Q2 plus enough voltage to keep them out of saturation.

Many design variations exist to decrease drop out voltage such as using a PNP or FET device for Q1. Typically these techniques raise the regulator's output impedance by a factor of 10 or more, which again limits dynamic response.

A New Generation Regulator

Design

Some modern regulators have innovations to help them overcome some of the limitations we just discussed, but typically their best PSRR is over a fairly limited bandwidth, their transient step performance is mediocre and/or they have relatively high noise. The patented Belleson design steps beyond performance levels of the older and the more modern designs.

The Belleson design is an evolution of a design from Philbrick ca. 1961 by Bob Pease[1], one by John Roberts in 1985[2], and one by Walt Jung in 2000[3]. The common factor among these designs is that they power the voltage reference and the error amplifier with the regulator's own output voltage.

Looking at figure 1 again, consider if A1's positive supply connection was to VOUT instead of VIN. To control Q1, A1's output must reach VOUT+ Q1's V_{BE}, which is above A1's positive supply—it won't work.

To make it work, a level shifter is necessary. Belleson's innovation is to use a JFET's negative V_{GS} to shift the control voltage level down to within A1's output voltage range. Figure 2 illustrates how, with proper selection of J1, A1 operates within its power supply range while controlling the loop.

Now there are no current sources connected to VIN. In fact only two components are connected to VIN, both via their high impedance nodes. All other paths for VIN AC noise to make its way to VOUT are gone and both J1 and Q1 have the benefit of being inside the error correction feedback loop.

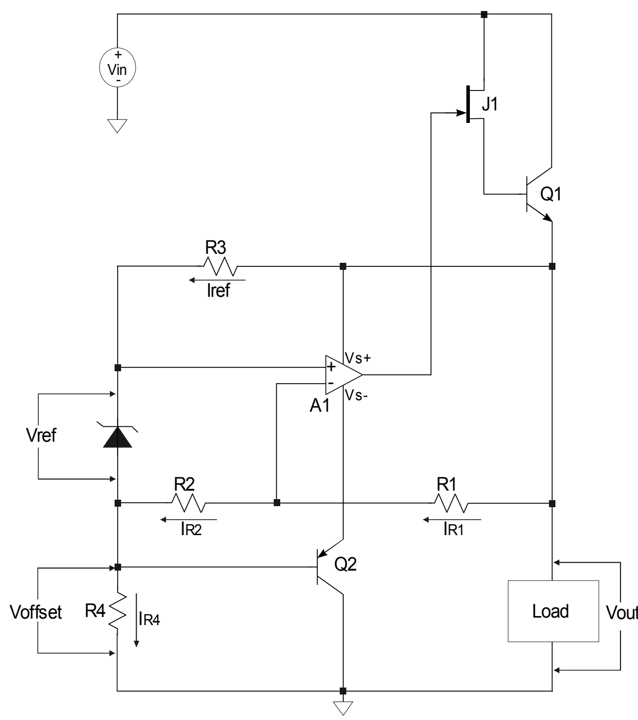

Figure 2: Belleson self powered regulator.

The reference is also powered by VOUT, and by using (VOUT – VREF)/R3 to set a fixed current through the reference, there exists a fixed current sum equal to $I_{R3} + I_{R2}$. This reference current is passed through resistor R4 to offset the entire regulation apparatus from ground and float VOUT to any value within the breakdown voltage of Q2. Floating the control circuit allows it to operate with a fixed voltage between the bottom side of VREF and VOUT, with A1 at a fixed low gain for maximum bandwidth.

Self powered regulators can have start–up problems[3], however with a sufficiently low R3 to allow the reference to reach its specified voltage (necessary for normal operation anyway) this design has a starting current path through the resistive J1 channel, Q1 VBE, R3, VREF and R4 to ensure proper start up.

Drop out voltage is the forward V_{BE} of Q1 plus the V_{DS} of J1, which can be as low as 0.8 to 2 volts depending

1.http://archive.electronicdesign.com/files/29/1509/figure_01.gif
2.Roberts, John H. *The Preeminent* Preamp, The Audio Amateur, 3/85.
3.http://waltjung.org/PDFs/Improved_PN_Regs.pdf

on Q1 and output current. While not as low as the Vsat of a single PNP pass device or the Vds(on) of a MOSFET, drop out voltage is quite low compared to many available regulators.

PSRR Measurements

With only two connections to VIN, it's clear there are fewer paths for unwanted input AC to get to VOUT, and the two connections are both high impedance—J1 drain and Q1 collector. This gives improved supply rejection compared to other available regulators as shown in figures 3 and 4, which show PSRR for a set of commercially available regulators.

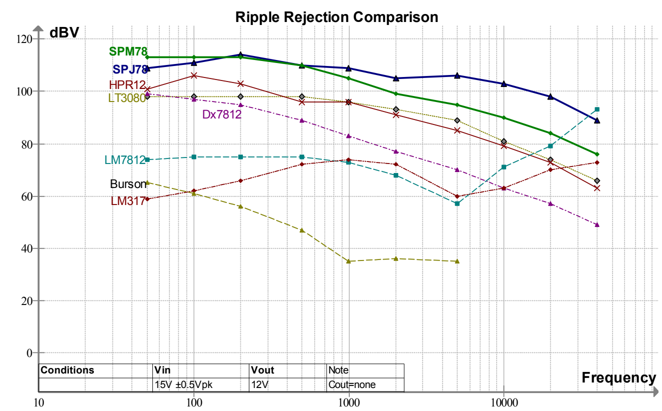

Figure 3: PSRR vs. frequency, 50Hz to 100KHz, Cout=none

Measurements for figure 3 were taken with no capacitor added to the regulator output, figure 4 measurements use a 100µF capacitor. All measurements were taken in the same test setup with the same equipment.

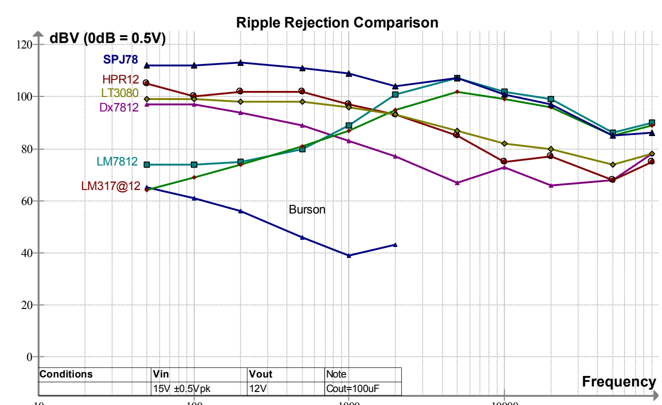

Figure 4: PSRR vs. frequency, 50Hz to 100KHz, Cout=100µF

Notice that the output capacitor greatly improves the supply rejection of monolithic regulators such as LM317 and LM7812 as frequency increases. Measurements used a capacitor at any adjust pin as specified by their respective data sheets.

Load Regulation

The extent to which a regulator can keep its output voltage constant with a changing load is its load regulation. DC or static load regulation is typically measured by monitoring Vout at two different DC load currents and taking their ratio. However, this measurement is not useful in a real world situation where the load can change by large relative amounts in a very short time. This type of AC load regulation is known as *load transient response* or dynamic performance. Dynamic performance is one of the most important and overlooked characteristics of a voltage regulator.

When an amplifier must supply a large fast current to a load, whether the load is a speaker, a capacitive cable or data converter, if the regulator output changes then transient response is compromised and the signal can be distorted. Not only will the part of the signal that caused the transient distortion be affected, but all signal components that exist while the regulator recovers will be affected.

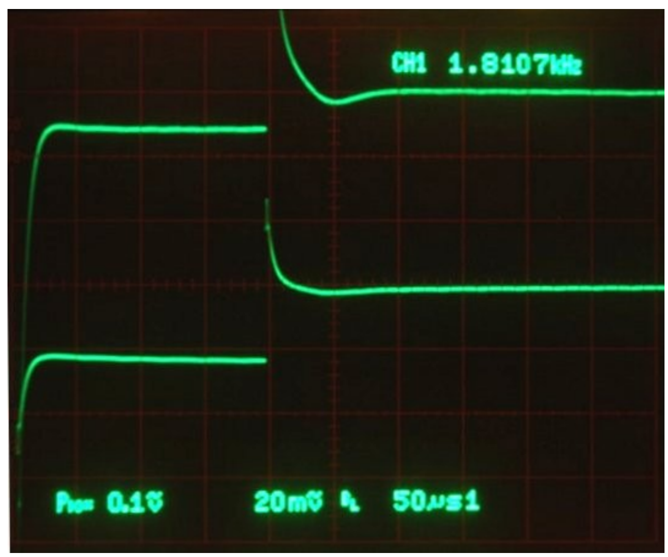

Figure 5: LM7812 load transient response, 1A current step.

Consider a standard monolithic voltage regulator such as the LM7812. When a 1 amp current pulse is demanded from the output, what happens? The oscillograph in figure 5 shows the output voltage (top trace) and the load current as 0.1V/0.1Ω per division (bottom trace).

The LT3080 output response is shown in figure 6, to illustrate a more recent (and award winning) design from Linear Technology.

http://www.belleson.com/

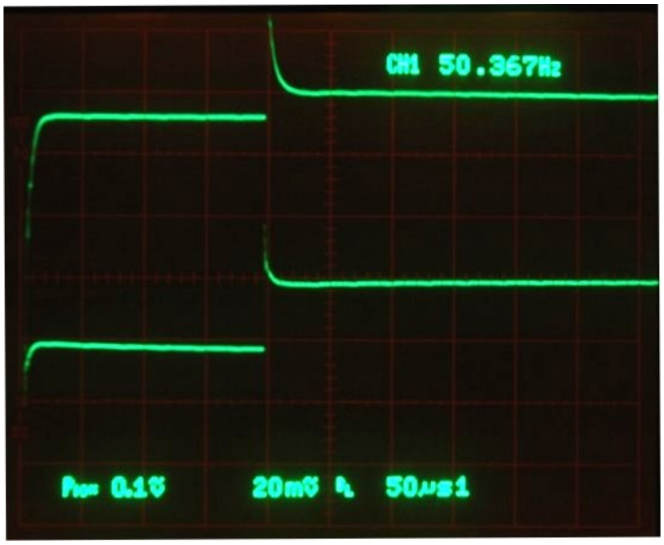

Figure 6: LT3080 load transient response, 1A current step.

This is a strident test for a linear voltage regulator. It demonstrates how the regulator might respond to a load with digital circuitry such as a clock. A slow response may not cause a logic level error, but could increase clock jitter by delaying signal transitions. This is particularly critical in high resolution or high speed data converters and high data rate signal transceivers.

Contrast these results to the same test done on a Superpower in figure 7. Notice the exceptionally small transients when the current goes from 10mA to 1A and again when it goes from 1A back to 10mA.

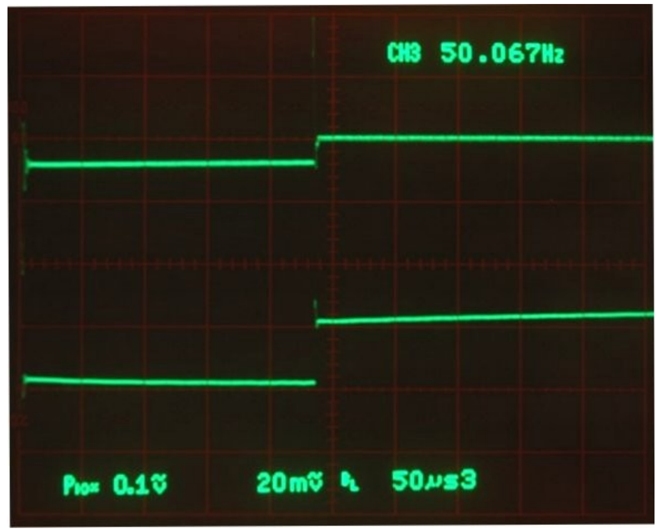

Figure 7: SPJ78 load transient response , 1A load current step.

Figure 8 shows the step response of a Belleson SPM78 12V regulator, which is a TO-220 size PCB that delivers up to 225mA. Note that all load transient step tests were done with a 100μF electrolytic capacitor at the regulator output.

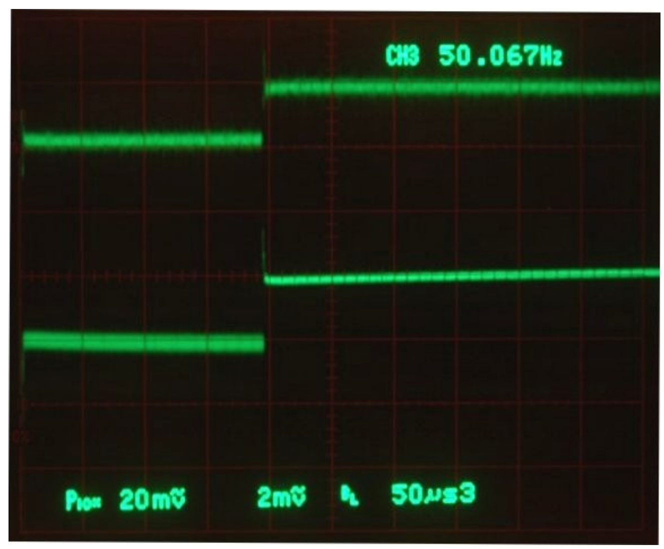

Figure 8: SPM78 load transient response, 200mA load current step.

Noise

The effect of power supply noise on a load circuit can be more or less depending on the circuit. To the extent that its differential halves match, a fully differential circuit cancels power supply noise by making it common to both halves. At the other extreme a single ended resistively loaded amplifier stage will pass power supply noise directly to the next stage.

It's easy to agree that low noise in a regulator is a worthy goal, and Superpower is one of the lowest noise voltage regulators available, with RMS noise of less than 1 PPM of Vout. SPJ measures <10µVrms (20Hz-20kHz) for a 12V output Superpower, making it ideal for use in low level subsystems such as microphone amplifiers, phono stages, preamplifiers, DACs, ADCs, digitizers, sensor amplifiers etc. The noise floor spectrum is shown in figure 8.

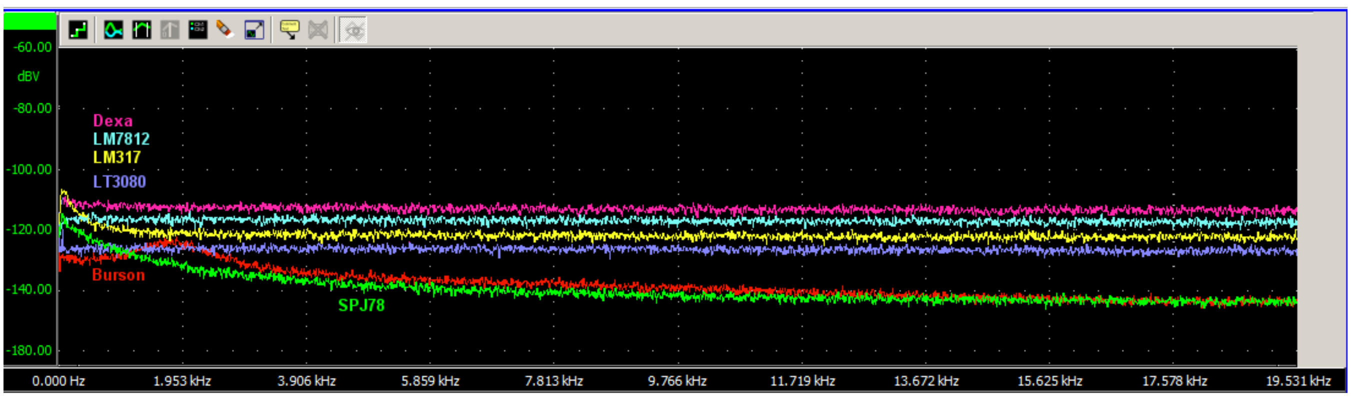

Figure 9: Noise measurement of several regulators

Conclusion

Standards for voltage regulator performance have been raised in a new regulator design from Belleson LLC. Belleson's patented Superpower voltage regulators offer the following benefits over others:

- Higher current
- Higher voltage
- Higher ripple rejection
- Faster transient step response
- Lower noise

If your requirements demand the very best performance, choose Superpower™.

Belleson

http://www.belleson.com/